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REMARKS

Several minor changes have been made to the specification. A spelling/grammatical error has been corrected in paragraph 21. The parenthetical reference to application Fig. 7A after the reference to isolation trenches 560 in the first sentence of the paragraph 38 has been deleted since none of trenches 560 appears in Fig. 7A. In paragraph 42, the sentence which specifies that the aspect ratio is 1.6 to 2.5 and which immediately follows the sentence providing that the width of cobalt silicide line 210 is approximately 0.13 - 0.21 μm has been deleted since (a) "aspect ratio" means the ratio of the height of an opening to its (minimum) width at the bottom of the opening and (b) the width at the bottom of an opening having cobalt silicide line 210 is indicated in Fig. 7B as being significantly greater than the width of line 210.

Claims 8 - 25 have been added. No claims have been amended or canceled. Accordingly, Claims 1 and 3 - 25 are now pending.

Claims 1, 3, 4, and 7 have been rejected under 35 USC 103(a) based on Blair, U.S. Patent 6,136,705, in view of Venkatraman et al. ("Venkatraman"), U.S. Patent 6,093,066, and Chiang et al. ("Chiang"), U.S. Patent Publication 2002/0132473 A1. This rejection is respectfully traversed.

Blair discloses a "salicidation" technique in which cobalt layer 118 is deposited on a semiconductor structure, including the silicon source, drain, and gate electrodes of an insulated-gate field-effect transistor. Titanium layer 120 is deposited on cobalt layer 118. At col. 4, lines 49 - 50, Blair specifies that the deposition of titanium layer 120 is performed "using conventional sputtering techniques".

Blair then reduces the titanium thickness at selected areas, including above the gate electrode, of layer 120. A rapid thermal anneal ("RTA") is conducted to convert the cobalt into cobalt silicide along the areas, including the source, drain, and gate electrode, where cobalt layer 118 directly contacts silicon. Blair subsequently removes the remainder of titanium layer 120 and any unreacted cobalt. In the resultant structure, the cobalt silicide is thicker at the areas where the thickness of titanium layer 120 was reduced than at other areas.

Venkatraman discloses an opening-filling technique in which a barrier layer consisting of silicon, nitrogen, and one or more refractory metals is deposited by ionized physical vapor deposition ("IPVD") in two stages on a semiconductor structure and into openings in the

structure to line the openings with a barrier layer. The first stage of the barrier-layer deposition is performed at a lower bias than the second stage. At col. 5, lines 48 - 51, Venkatraman specifies that "the first stage bias can be kept close to zero".

One of the refractory metals cited by Venkatraman as a candidate for the barrier layer is titanium. In addition to silicon and nitrogen, Venkatraman's barrier layer may thus include titanium. Venkatraman subsequently deposits copper on top of the structure and into the openings to fill the remainder of each opening with copper. A planarization operation is performed to remove copper extending out of the openings.

Chiang discloses an opening-filling technique in which chemical vapor deposition ("CVD") or/and physical vapor deposition ("PVD"), such as IPVD, is utilized to deposit one or more barrier layers consisting of tantalum, tungsten, tantalum nitride, or tungsten nitride on a semiconductor structure and into openings in the semiconductor structure down to silicon at the bottom of the openings in order to line the openings with the barrier material. The structure is heated to form tantalum silicide or tungsten silicide at the locations where the barrier metal contacts silicon. Copper is subsequently deposited over the structure and into the openings to fill the remainder of each opening with copper. At paragraph 32, Chiang discloses that IPVD can be performed with a PVD chamber having an AC power source coupled to the semiconductor structure.

Claim 1, as revised in the Amendment submitted 18 September 2002, recites:

> 1. A method for forming cobalt silicide on a body which has a surface that comprises silicon, the method comprising:
>
> forming a cobalt layer on said surface;
>
> forming a titanium layer over the cobalt layer by ionized physical vapor deposition while the body is attached to a support biased with an AC power of 0 W;
>
> reacting the cobalt with the silicon to form cobalt silicide; and
>
> removing the titanium layer, and if any cobalt has not reacted with the silicon then removing the unreacted cobalt.

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At page 3 of the present Office Action, the Examiner begins a discussion directed to show that Claims 1, 4, and 7 are obvious based on Blair, Venkatraman, and Chiang. The Examiner first notes that "Blair fails to teach utilizing an ionized physical vapor deposition (IPVD) for forming the titanium layer while the body is attached to a support biased with an

AC power of 0 W". The Examiner then alleges that Venkatraman teaches "utilizing the IPVD for forming the titanium layer (col.5, lines 28-38), wherein the forming step is performed at the bias power of close to zero W (col.5, lines 48-50) for the purpose of preventing the adjacent layers from damage (col.6, lines 4-6)" and that it therefore "would have been obvious to one of ordinary skill in the art at the time of invention was made to utilize the IPVD method with the body attaching to a support biased with a power of 0 W as taught by Venkartraman [sic, Venkatraman] et al. for forming the titanium layer of Blair".

The Examiner next observes that "the combined teachings of Blair and Venkartraman et al. do not expressly teach that the power source is AC". After stating the Chiang teaches "that the bias power source is typically an AC source (section [0032])", the Examiner concludes the obviousness discussion with the allegation that it therefore "would have been obvious to one of ordinary skill in the art at the time of invention was made to form the titanium layer of Blair utilizing the IPVD method with the body attaching to a support biased with a power of 0 W as taught by Venkartraman et al., wherein the bias power can be the AC source as taught by Chiang et al., since this is a typical operation in IPVD method".

Claim 1 recites a <u>titanium</u> layer. <u>Contrary</u> to what the Examiner alleges, Venkatraman does <u>not</u> disclose the formation of a <u>titanium</u> layer, whether by IPVD or by any other technique.

More particularly, Venkatraman's barrier layer is formed by IPVD. As mentioned above, one of the candidate metals for use in Venkatraman's barrier layer is titanium. However, Venkatraman's barrier layer <u>also</u> contains <u>silicon and nitrogen</u>. See col. 5, lines 22 - 26, where Venkatraman states that "copper barrier layer 200 is typically a tantalum silicon nitride layer, but may also be composed of any combination of refractory metal such as molybdenum, tungsten, titanium, vanadium <u>together</u> with <u>silicon</u> and <u>nitrogen</u> [emphasis added] (e.g. a nitrogen-containing tantalum)". The amounts of silicon and nitrogen in Venkatraman's barrier layer appear to be substantial. Hence, Venkatraman's barrier layer is <u>not</u> the titanium layer of Claim 1.

Aside from the barrier layer, Venkatraman does not appear to disclose any layer which contains titanium and which is formed by IPVD. Since Venkatraman's barrier layer is not the IPVD-formed titanium layer of Claim 1, Venkatraman <u>fails</u> to disclose the IPVD-formed titanium layer of Claim 1.

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Neither Blair nor Chiang discloses the use of IPVD to form a titanium layer. Since Venkatraman does not utilize IPVD to form a titanium layer, the combination of Blair, Venkatraman, and Chiang would not teach the full subject matter of Claim 1 even if there were some motivation or suggestion for combining the three references in the manner proposed by the Examiner. Accordingly, Claim 1 is patentable over Blair, Venkatraman, and Chiang.

In addition, Venkatraman employs its barrier layer to prevent subsequently deposited electrically conductive material, i.e., copper, from diffusing into the underlying material and damaging the resultant semiconductor device. In the invention of Claim 1, the titanium layer is removed subsequent to formation of cobalt silicide from the earlier-deposited cobalt layer. Hence, the titanium layer in Claim 1 is absent when any further material is deposited over the structure produced according to the method of Claim 1 and, unlike Venkatraman's barrier layer, cannot prevent any such further deposited material from diffusing into the underlying material and damaging the resultant semiconductor device.

In other words, Venkatraman employs its barrier layer for a materially different purpose than that for which the titanium layer is utilized in the invention of Claim 1. Accordingly, there would be no reason for applying the teachings of Venkatraman to the teachings of Blair, and thus no reason for combining Blair, Venkatraman, and Chiang. This is a separate reason why Claim 1 is patentable over the three references.

Claims 3, 4, and 7 depend from Claim 1. Consequently, dependent Claims 3, 4, and 7 are patentable over Blair, Venkatraman, and Chiang for the same reasons as Claim 1.

Claims 5 and 6 have been rejected under 35 USC 103(a) as obvious based on Blair in view of Venkatraman and Chiang and further in view of Venkatesan et al. ("Venkatesan"), U.S. Patent 5,863,598, and Givens, U.S. Patent Publication 2002/0019127. This rejection is respectfully traversed.

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Venkatesan discloses a technique for depositing polycrystalline silicon or/and amorphous silicon into openings having an aspect ratio of 2 or more. The aspect ratio is 2.5 in one example in Venkatesan.

Givens discloses depositing titanium into a contact opening down to silicon at the bottom of the opening by PVD or CVD, annealing to absorb oxygen of the native silicon oxide layer into the titanium (apparently without forming a titanium silicide bottom layer or a

titanium nitride top layer), depositing cobalt, annealing to cause cobalt to move through the titanium and oxygen to form a cobalt silicide layer, removing the titanium, oxygen, and unreacted cobalt, depositing titanium, depositing titanium nitride, and finally depositing a tungsten interconnect layer. The cobalt silicide forms one diffusion barrier, and the titanium/titanium nitride layer forms another diffusion barrier.

Claims 5 and 6 both depend from Claim 1. Hence, each of Claims 5 and 6 contains all the subject matter of Claim 1. As mentioned above, the combination of Blair, Venkatraman, and Chiang would not teach the full subject matter of Claim 1 even if there were some suggestion or motivation for combining the three references in the proposed manner. Neither Venkatesan nor Givens fills this deficiency in the teachings of Blair, Venkatraman, and Chiang.

As also mentioned above, nothing in Blair, Venkatraman, and Chiang would provide a person skilled in the art with any motivation or suggestion for combining the three references. Venkatesan and Givens likewise do not provide any motivation or suggestion for combining Blair, Venkatraman, and Chiang. Claims 5 and 6 are thus patentable over Blair, Venkatraman, Chiang, Venkatesan, and Givens for the same reasons that Claim 1 is patentable over Blair, Venkatraman, and Chiang.

New Claim 8, presented below, is an independent claim that largely repeats the subject matter of the originally filed version of Claim 1:

> 8. A method comprising:
>
> forming a cobalt layer over a body that comprises silicon;
>
> forming a titanium layer over the cobalt layer by ionized physical vapor deposition;
>
> reacting cobalt of the cobalt layer with silicon of the body to form a cobalt silicide layer; and
>
> substantially removing the titanium layer and any unreacted cobalt of the cobalt layer.

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Due to the close connection between Claim 8 and the originally filed version of Claim 1, Applicants' attorney will first address the reasons presented in the previous Office Action, mailed 14 August 2002, for rejecting the originally filed version of Claim 1. In that Office Action, Claim 1 was rejected under 35 USC 103(a) as obvious based on Blair in view of Cerio, U.S. Patent 6,268,284. After noting that "Blair fails to teach utilizing an ionized

physical vapor deposition (IPVD) for forming the titanium layer", the Examiner alleged on page 3 of the 14 August 2002 Office Action that "using the IPVD for forming titanium layer is a well-known method, as evidenced by Cerio (abstract)" and that it therefore it "would have been obvious to one of ordinary skill in the art at the time of invention was made to utilize the IPVD as taught by Cerio for forming the titanium layer of Blair since this deposition method would provide a better wetting layer for subsequent deposition and improve layer thickness control (see abstract)".

Cerio discloses the deposition of a layer formed with two elements, at least one of which is a metal, by IPVD to form a composite layer with improved wetting characteristics for subsequent metal deposition. Cerio's IPVD-formed layer is typically titanium aluminide, referred to as "$TiAl_3$" at numerous places in Cerio's specification. At the bottom of col. 3, Cerio indicates that the IPVD-formed layer can alternatively consist of titanium-tungsten or titanium silicide.

Claim 8 recites a titanium layer. Similar to what was said above about Venkatraman and contrary to what the Examiner alleges, Cerio does not disclose forming a titanium layer, whether by IPVD or by any other technique. Instead, Cerio discloses the use of IPVD to form a layer consisting of (a) titanium and (b) aluminum, tungsten, or silicon.

As evidenced by the stoichemetric formula "$TiAl_3$" used by Cerio to identify the titanium aluminide layer, the amount of aluminum in Cerio's titanium aluminide layer is substantial. Likewise, the amount of tungsten in Cerio's titanium-tungsten layer appears to be substantial, and the amount of silicon in Cerio's titanium silicide layer appears to be substantial. Consequently, Cerio's IPVD-formed layer is not the titanium layer of Claim 8.

As mentioned above, Blair does not disclose the use of IPVD to form a titanium layer. Inasmuch as Cerio does not disclose the use of IPVD to form a titanium layer, the combination of Blair and Cerio would not teach the full subject matter of Claim 8 even if there were some suggestion or incentive for combining Blair and Cerio in the proposed manner. Claim 8 is thus patentable over Blair and Cerio.

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Similar to Venkatraman, Cerio employs its IPVD-formed layer as a barrier layer over which electrically conductive material for an electrical interconnect system is deposited. The materials that form Cerio's IPVD-formed barrier layer are chosen to facilitate deposition and adhesion of the subsequently deposited conductive interconnect material. Conversely, the

titanium layer in the invention of Claim 8 is removed subsequent to the formation of cobalt silicide from the earlier-deposited cobalt layer. The titanium layer of Claim 8 is absent when any further material is deposited over the structure produced according to process of Claim 8.

Similar to what was said above about Venkatraman with respect to Claim 1, Cerio thus utilizes its IPVD-formed layer for a materially different than the purpose for using the titanium layer in the invention of Claim 1. There would be no reason for applying the teachings of Cerio to Blair's teachings. This is a separate reason why Claim 8 is patentable over Blair and Cerio.

As to the combination of Blair, Venkatraman, and Chiang applied against Claim 1, Claim 8 is patentable over Blair, Venkatraman, and Chiang for the same reasons as Claim 1.

Claims 9 - 25 all depend (directly or indirectly) from Claim 8. As a result, Claims 9 - 25 are patentable over Blair and Cerio, separately or in combination with Venkatesan or/and Givens, for the same reasons that Claim 8 is patentable over Blair and Cerio. Claims 9 - 25 are also patentable over Blair, Venkatraman, and Chiang, separately or in combination with Venkatraman or/and Givens, for the same reasons that Claim 8 is patentable over Blair, Venkatraman, and Chiang.

In addition, none of the applied references discloses the further limitation of any of dependent Claims 23 - 25. This establishes a separate basis for allowing Claims 23 - 25 over the applied references.

In summary, Claims 1 and 3 - 25 have been shown to be patentable over the applied references. Accordingly, Claims 1 and 3 - 25 should be allowed so that the application may proceed to issue.

Please telephone Applicants' attorney at 650-964-9767 if there are any questions.

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Ronald J. Meetin — 4 March 03

Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

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PARAGRAPHS 21, 38, AND 42, WITH ANNOTATIONS TO INDICATE REVISIONS, OF SPECIFICATION OF U.S. PATENT APPLICATION 10/056,154, ATTY DOCKET. NO. M-12524 US

[0021] Then titanium layer 130 is deposited by ionized PVD. In some embodiments, the titanium is deposited *in-situ*, without breaking the vacuum after the cobalt deposition and without unloading the wafer from the Endura cluster tool, and the deposition is performed in a medium throw magnetron IMP (ion metal plasma) chamber 410 (Fig. 4) of type Vectra available as part of the Endura tool. Titanium target 420 is shown mounted at the top of chamber 410. Target 420 is connected to a negative DC bias source 430. Wafer 102 is placed on a metallic pedestal 440. Bias source 450 biases the pedestal with an AC current of a frequency 13.56MHz. Argon is **flowed** [flown] into the chamber. Bias source 430 helps ionize the argon. Coil 460 generates an RF electromagnetic field to densify the argon plasma, making the plasma high density. The argon ions dislodge titanium atoms from target 420. Some of the titanium atoms become ionized by the high density plasma. The titanium atoms and ions settle on wafer 102. See "Handbook of Semiconductor Manufacturing Technology" (edited by Yoshio Nishi et al., 2000), pages 395-413, incorporated herein by reference.

[0038] Isolation trenches 560 (Figs. 6 **and** [, 7A,] 7B) in substrate 104 are filed with dielectric 564 ("field oxide"), which is silicon dioxide in some embodiments. Dielectric 564 provides isolation between the active areas of the memory array. The trench boundaries are shown at 560B in Fig. 6. The trenches extend in the bitline direction between adjacent source lines 544. Each trench 560 passes under two rows of the array and projects from under the respective control gate lines 528 into the source lines.

[0042] In the cross section of Fig. 7B, the height of each stack 532 is about 0.3 μm. The width of the cobalt silicide line 210 is about 0.13 μm to 0.21 μm. [The aspect ratio is thus about 1.6 to 2.5.] The width of each dielectric feature 534 at the bottom is about 0.02 μm to 0.06 μm.

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